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10/672,972	09/26/2003	Masakatsu Uneme	N28733102E	3617

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,972	UNEME, MASAKATSU	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Remarks filed on July 11, 2006 regarding application 10,672,972 filed on September 26, 2003.

2. Claims 1-21 are pending in the application under consideration.

3. ***Response to Remarks***

Applicant's remarks have been fully and carefully considered with the Examiner's response set forth below.

Response to remark on Claim Rejections - 35 USC § 112 regarding "linearly aligned"

Applicant contends that the term "linearly aligned" has ordinary and customary meanings and provides a number of examples as explanation. However, they fail to address the issue that the Examiner raised in the previous Office Action for the following reasons:

First, the 35 USC 112 rejections are directed to claims 2 and 20 because they recite the limitation of "**linearly aligned**" between two sets of signals (the m data output terminals and the n signal output terminals). However, it is not clear as to what constitutes being "**linearly aligned**." The Specification section of the Application fails to provide a definition of this term, and it is difficult to comprehend how "m" terminals are "**linearly aligned**" to "n" terminals.

It should be noted that while it is clear how one set of objects is linearly aligned (they form a line), it is not clear how two sets of objects (the set of "m" terminals and the second set of "n" terminals) are linearly aligned. Does it mean that each set of the

objects form its respective line? Or all of the objects of the two sets have to form a single line? Or each set of the objects form its respective line, and the two lines have to have certain relationship, such as parallel to each other or a particular angle?

Second, Applicant cited paragraph [0075] of the Application to support the term

"Also, as shown in FIG. 3, "n" input delay circuits 111 and "n/2" output delay circuits 112, including a DLL, and the like, can be arranged between the linear aligned data/signal I/O terminals (105/106) and linear aligned first stage and final stage FFs (107/108)"

However, the paragraph merely states that the data/signal I/O terminals (only one set of objects) are linearly aligned, and that he FFs (one set of objects) are linearly aligned. This paragraph shows examples of "one set of objects" are linearly aligned, but fails to provide even an example how "two sets of objects" are linearly aligned.

Third, merely showing an example is not sufficient to define the scope and bound of a claim limitation (because there may be other different examples that are also considered as "linearly aligned"), which is critical to the determination of the merits of a claim regarding its patentability. This is particularly important in light of Applicant's remark that "**Importantly, the above examples should not necessarily be construed as limiting to Applicant's invention. The examples represent but particularly embodiments of the invention**."

Thus, one the one hand, Applicant wishes to use a mere example as substitution of "definition" of a critical term recited in the claim, and on the other hand wishes not to be limited to that "definition." This makes assessing the scope and bound of a claim limitation difficult, if not impossible.

Fourth, Applicant contends that the term "linearly aligned" is also understood from the prior art and provides the following three examples for illustrations:
US Patent 7,067,876, Col. 18, Lines 39-41, which shows "the drain layers 70 are linearly aligned in parallel with the line E-E' under the drain electrodes 20." Note that it recites "linearly aligned **in parallel**,' and not simply "linearly aligned."
US Patent 7,027,334, Col. 3, Lines 53-55, which shows "a bitline 19 is connected through a contact plug 18 to the drain diffusion layer 16b of each of linearly aligned of

"queued" memory cells MC ..." Note that it recites that the memory cells MC are linearly aligned, which is only one set of objects, not "two sets of objects" being linearly aligned. US Patent 6,841,417, Col. 7, Lines 23-25, which shows "the longitudinal member 234 are uniformly and linearly aligned with a longer diagonal line L." Note that it recites that one sets of objects, the longitudinal member 234, being linearly aligned, and not "two sets of objects" being linearly aligned.

Therefore, the Examiner's position regarding the 35 USC 112 rejections to claims 2 and 20 remain as the same.

Response to other remarks

In response to these remarks, a new ground of claim analysis based on Applicant's admission of prior art (Uneme, US Patent Application Publication 2004/0076002 A1) and in view of Ahuja (US 5,307,381) has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2 and 20 recite the limitation of "**linearly aligned**" between two sets of signals (the m data output terminals and the n signal output terminals). However, it is not clear as to what constitutes being "**linearly aligned**." The Specification section of

the Application fails to provide a definition of this term, and it is difficult to comprehend how "m" terminals are "**linearly aligned**" to "n" terminals.

Applicant contends that the term "linearly aligned" has ordinary and customary meanings and provides a number of examples as explanation. However, they fail to address the issue that the Examiner raised in the previous Office Action for the following reasons:

First, the 35 USC 112 rejections are directed to claims 2 and 20 because they recite the limitation of "**linearly aligned**" between two sets of signals (the m data output terminals and the n signal output terminals). However, it is not clear as to what constitutes being "**linearly aligned**." The Specification section of the Application fails to provide a definition of this term, and it is difficult to comprehend how "m" terminals are "**linearly aligned**" to "n" terminals.

It should be noted that while it is clear how one set of objects is linearly aligned (they form a line), it is not clear how two sets of objects (the set of "m" terminals and the second set of "n" terminals) are linearly aligned. Does it mean that each set of the objects form its respective line? Or all of the objects of the two sets have to form a single line? Or each set of the objects form its respective line, and the two lines have to have certain relationship, such as parallel to each other or a particular angle?

Second, Applicant cited paragraph [0075] of the Application to support the term

"Also, as shown in FIG. 3, "n" input delay circuits 111 and "n/2" output delay circuits 112, including a DLL, and the like, can be arranged between the linear aligned data/signal I/O terminals (105/106) and linear aligned first stage and final stage FFs (107/108)"

However, the paragraph merely states that the data/signal I/O terminals (only one set of objects) are linearly aligned, and that he FFs (one set of objects) are linearly aligned. This paragraph shows examples of "one set of objects" are linearly aligned, but fails to provide even an example how "two sets of objects" are linearly aligned.

Third, merely showing an example is not sufficient to define the scope and bound of a claim limitation (because there may be other different examples that are also considered as "linearly aligned"), which is critical to the determination of the merits of a claim regarding its patentability. This is particularly important in light of Applicant's remark that "**Importantly, the above examples should not necessarily be construed as limiting to Applicant's invention. The examples represent but particularly embodiments of the invention**."

Thus, one the one hand, Applicant wishes to use a mere example as substitution of "definition" of a critical term recited in the claim, and on the other hand wishes not to be limited to that "definition." This makes assessing the scope and bound of a claim limitation difficult, if not impossible.

Fourth, Applicant contends that the term "linearly aligned" is also understood from the prior art and provides the following three examples for illustrations:
US Patent 7,067,876, Col. 18, Lines 39-41, which shows "the drain layers 70 are linearly aligned in parallel with the line E-E' under the drain electrodes 20." Note that it recites "linearly aligned **in parallel**,' and not simply "linearly aligned."
US Patent 7,027,334, Col. 3, Lines 53-55, which shows "a bitline 19 is connected through a contact plug 18 to the drain diffusion layer 16b of each of linearly aligned of

"queued" memory cells MC ..." Note that it recites that the memory cells MC are linearly aligned, which is only one set of objects, not "two sets of objects" being linearly aligned.

US Patent 6,841,417, Col. 7, Lines 23-25, which shows "the longitudinal member 234 are uniformly and linearly aligned with a longer diagonal line L." Note that it recites that one sets of objects, the longitudinal member 234, being linearly aligned, and not "two sets of objects" being linearly aligned.

Therefore, as far as the determination of the patentability is concerned, the term "linearly aligned" remains undefined.

6. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation of "each m output holding circuit is **physically adjacent to** a corresponding one of the m data output terminals;" and "the output of each output delay circuit is **adjacent to** the corresponding p signal output terminals(s)."

First, is there a difference between being "**physically adjacent to**" as opposed to being simply "**adjacent to**?"

Second, the American Heritage College Dictionary defines the word "adjacent" as "close to or near to." The question is how close/near is considered as being close to (near to). Is it 1 centimeter? Is it 1 millimeter? Or is it 1 micrometer? Clarification is needed.

7. Claims 8 and 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8, 14 and 15 each recites the limitation of "the length of wiring being **essentially** equal."

First, is there a difference between being "**essentially** equal" as opposed to being simply "equal?"

Second, a question arises as to how two lengths are considered as being "essentially equal." Is it within 1 centimeter? Is it within 1 millimeter? Or is it within 1 micrometer? Clarification is needed.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art (Uneme, US Patent Application Publication 2004/0076002 A1), and in view of Ahuja (US 5,307,381).

As to claim 1, Applicant's admission of prior art discloses **a memory controller connected to a semiconductor memory device** [figures 10-12 (background art); paragraphs 0004~0023 describe the internal configuration as well as the write/read operations to/from a memory device by a conventional memory controller], **comprising**:

a clock generating circuit that generates an output clock signal [figure 10, 212; Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); Clock generating

circuit 212 is composed of a phase locked loop (PLL) circuit to generate the output clock signal (paragraph 0011)];

a data generating circuit that provides output digital data [Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); paragraphs 0015~0016];

a predetermined number "m" data output terminals that provide output data to the semiconductor memory device in parallel [Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); figure 10, 215 shows a predetermined number of data output terminals];

m output holding circuits for storing the output digital data synchronously with the output clock signal [Referring to FIGS. 10 and 11, in the following description, it

will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); Referring to FIG. 10, memory controller 200 stores data in data storing circuit 211. Write data stored therein can be provided to final stage FFs 218. Such write data can be output to the DDR-SDRAM through wirings 225 and data I/O terminals 215. In the write operation, a clock signal can be input to clock terminals final stage FFs 218. Such a clock signal can be obtained by skew adjusting the clock signal generated by clock generating circuit 212 using clock tree synthesis (CTS). Thus, all final stage FFs 218 used to write data, hold such data at the same time for output to data I/O terminals 215 (paragraph 0009); figure 10, 218 shows a predetermined number of final stage FFs];

a predetermined number "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where n<m [figure 10, 212; Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O)

terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); One signal I/O terminal 216 can be provided for each predetermined group of data I/O terminals (e.g., every 8 bits) (paragraph 0012)]; **and a plurality of output delay circuits including one output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s)** [figure 10, 212; Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009); The output delay circuit 213 can receive as an input the clock signal from clock generating circuit 212 and output a delayed clock signal, which is obtained by delaying the clock signal by a predetermined amount (e.g., a quarter cycle) (paragraph 0011); paragraph 0018];

wherein each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals [figure 10]; **and**

the output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) [figure 10].

Regarding claim 1, Applicant's admission of prior art teaches the configuration that "one output delay circuit for every "p" signal output terminal(s)" as recited in the claim, but does not mention "a plurality of output delay circuits."

However, it is well known in the art that every electronic circuit has a "fan-out" limitation that restricts the number of loads that it can support; and as the number of loads exceed the "fan-out" (or driving) capability of a single circuit, a plurality of circuits must be used to ensure proper operations.

Further, Ahuja discloses in the invention "Skew-Free Clock signal Distribution Network in a Microprocessor" an apparatus [figures 1 and 2] that receives and delays an input clock signal via a plurality of delay circuits resides inside a "length equalizer" [figure 1, 14; figures 3-4; column 7, lines 19-41] and provides a plurality of delayed output clock signals, each to a group of logic circuits [figure 1, unit 1 through unit n; figure 2]. The length equalizer [figure 1, 14] equalizes the length of all clock lines [figure 1, 31-40n] such that the delay for the clock signal on each of the clock lines is equal [column 7, lines 19-41].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize the common and well-known practice of using a plurality of delay circuits to distributed a plurality of delayed clock signals to a plurality of groups of circuits in a skew-free manner, as demonstrated by Ahuja, hence the lack of patentable significance of this particular limitation.

As to claim 2, Applicant's admission of prior art teaches that **the m output data output terminals and n signal output terminals are linearly aligned with one another** [figure 10]; **the m holding circuits are linearly aligned with one another between m holding circuits and the aligned m data output terminals and n signal output signals** [figure 10].

As to claim 3, Applicant's admission of prior art teaches that **the memory controller of claim 1, wherein: the value p is greater than one, and the value n is a multiple of p** [figure 10, 216 shows a plurality of signal output terminal, thus p is greater than 1; figure 10, 215 also shows a plurality of data output terminal and that the number of data output terminal (n) is an integer multiple of the number of data output terminal (p)].

As to claim 4, Applicant's admission of prior art teaches that **the memory controller of claim 1, wherein: the value p is selected from the group consisting of one and two** [figure 10, 216 shows a plurality of signal output terminal, including the case where p may be one or two].

As to claim 5, Applicant's admission of prior art teaches that **the memory controller of claim 1, wherein: the value p is one** [figure 10, 216 shows a plurality of signal output terminal, including the case where p may be one or two].

As to claim 6, Applicant's admission of prior art teaches that **the value of p is two** [figure 10, 216 shows a plurality of signal output terminal, including the case where p may be one or two]; **and that each of the plurality of output delay circuits has an output terminal arranged equidistant from the corresponding two signal output**

terminals [it is assumed that the plurality of wirings 225 distributed between the final stage FFs 218 and data I/O terminals 215 can have the same length (paragraph 0017); Ahuja also teaches this aspect by using the length equalizer (figure 1, 14 and figures 3-4)].

As to claim 7, Applicant's admission of prior art teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 11, paragraphs 0013-0014 and 0020-0023];

a signal input terminal for every "q" data input terminals [figure 11 shows a strobe (216, signal input terminal) for a plurality (4) of data input terminals (215), q=4], **where "q" is an integer greater than 2** [q=4 as shown in figure 11], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [paragraphs 0013-0014 and 0020-0023];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 11, 219; paragraph 0014], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figure 11, 219]; **and an input holding circuit corresponding to each data input terminal** [figure 11, 220 and 217], **each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit** [figure 11]; **wherein the input data is**

transmitted to the data generating circuit through the data input terminals [figures 10 and 11].

As to claim 8, Applicant's admission of prior art teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 11, paragraphs 0013-0014 and 0020-0023];

a signal input terminal for every "q" data input terminals [figure 11 shows a strobe (216, signal input terminal) for a plurality (4) of data input terminals (215), q=4], **where "q" is an integer greater than 2** [q=4 as shown in figure 11], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [paragraphs 0013-0014 and 0020-0023];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 11, 219; paragraph 0014], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figure 11, 219]; **and an input holding circuit corresponding to each data input terminal** [figure 11, 220 and 217], **each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit** [figure 11]; **wherein the input data is transmitted to the data generating circuit through the data input terminals** [figures 10 and 11];

a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit [figure 11, 2211]; **and**
a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit [figure 11, 2212];
wherein the first and second wiring corresponding to each input holding circuit being essentially equal in length [it is assumed that the plurality of wirings 225 distributed between the final stage FFs 218 and data I/O terminals 215 can have the same length (paragraph 0017); Ahuja also teaches this aspect by using the length equalizer (figure 1, 14 and figures 3-4)].

As to claim 9, Applicant's admission of prior art teaches that **the m data output terminals are also data input terminals that receive input data from the semiconductor memory device in parallel** [figure 11 shows that the 8 data terminals DATA0~DATA7 are bidirectional, serving as both input and output directions]; **and the n signal output terminals are also signal input terminals for receiving device input clock signals from the semiconductor memory device in synchronism with the input data** [figure 10, 216 shows a plurality of signal I/O terminals, figure 11 shows that the signal terminals STROBE0 is bidirectional, serving as both input and output directions].

As to claim 10, Applicant's admission of prior art teaches that **the output holding circuits transmit output digital data synchronously with both a rising edge and a falling edge of the output clock signal** [In DDR-SDRAM, digital data can

be input to, or output from the DDR-SDRAM on both the rise and fall of a clock signal (paragraph 0003)].

As to claim 11, Applicant's admission of prior art teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 11, paragraphs 0013-0014 and 0020-0023];

a signal input terminal for every "q" data input terminals [figure 11 shows a strobe (216, signal input terminal) for a plurality (4) of data input terminals (215), q=4], **where "q" is an integer greater than 2** [q=4 as shown in figure 11], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [paragraphs 0013-0014 and 0020-0023];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 11, 219; paragraph 0014], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figure 11, 219]; **and an input holding circuit corresponding to each data input terminal** [figure 11, 220 and 217], **each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit** [figure 11, 219]; **wherein the input data is transmitted to the data generating circuit through the data input terminals** [figure 11];

wherein the input holding circuits transmit input data to the data generating circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal [digital data can be input to, or output from the DDR-SDRAM on both the rise and fall of a clock signal (paragraph 0003)].

As to claim 12, Applicant's admission of prior art teaches that **the semiconductor memory device being coupled to the memory controller by the m data output terminals and the n signal output terminals** [figure 10 shows a plurality of data output terminals (215) as well as a plurality of signal output terminals (216)].

As to claim 13, Applicant's admission of prior art teaches that **the memory controller of claim 1, further including: a circuit core region in which the clock generating circuit and data generating circuit are formed; and an interface region surrounding the circuit core region in which the data output terminals, output holding circuits, signal output terminals, and output delay circuits are formed** [Referring to FIGS. 10 and 11, in the following description, it will be assumed a memory controller 200 has a circuit core region 202 and an interface region 203 provided around the periphery of the circuit core region 202. A data storing circuit 211, a clock generating circuit 212, and an output delay circuit 213 can be formed within the circuit core region 202. Data input/output (I/O) terminals 215, signal I/O terminals 216, first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009)];

wherein each output holding circuit comprising a first latch circuit [first stage flip-flops (FFs) 217, final stage FFs 218, input delay circuits 219, and data delay circuits 220 are formed in an interface region 203 (paragraph 0009)].

As to claim 14, Applicant's admission of prior art teaches that **the data output terminals are data input/output (I/O) terminals** [figure 11 shows that the 8 data terminals DATA0~DATA7 are bidirectional, serving as both input and output directions];

the signal output terminals are signal I/O terminals [figure 10, 216 shows a plurality of signal I/O terminals, figure 11 shows that the signal terminals STROBE0 is bidirectional, serving as both input and output directions];

m input holding circuits corresponding to the data I/O terminals formed in the interface region [figures 10 and 11], **each input holding circuit comprising a second latch circuit** [figure 11] **connected to a corresponding data I/O terminal by a first wiring** [figure 11], **the input holding circuits holding input data in synchronism with a corresponding input strobe signal** [figure 11]; **and**

an input delay circuit connected to each signal I/O terminal by a second wiring [figure 11, 219], **each input delay circuit delaying a received device input clock from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal** [paragraph 0020-0023], **each input strobe signal being connected to a corresponding second latch circuit by a third wiring** [figure 11];

wherein the length of the first wiring to each second latch circuit is essentially equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit [it is assumed that the plurality of wirings 225 distributed between the final stage FFs 218 and data I/O terminals 215 can have the same length (paragraph 0017); Ahuja also teaches this aspect by using the length equalizer (figure 1, 14 and figures 3-4)].

As to claim 15, refer to "As to claim 1" and "As to claim 14."

As to claim 16, Applicant's admission of prior art teaches that **the input delay circuits are arranged between the signal input terminals and locations where the input delay circuits output the input strobe signals** [figure 11, 219].

As to claim 17, refer to "As to claim 8."

As to claim 18, refer to "As to claim 12."

As to claim 19, refer to "As to claim 13."

As to claim 20, refer to "As to claim 2."

As to claim 21, refer to "As to claim 1" and "As to claim 7."

10. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Yanagawa, (US Patent Application Publication 2001/0046163), "Memory System and memory Controller with Reliable Data Latch operation."
- Nelson et al., (US 5,258,660), "Skew-Compensated Clock Distribution System."

- Zumkehr, (US Patent Application Publication 2003/0005346), "System and Method for Delaying a Strobe Signal."
- Noda et al., (US Patent Application Publication 2001/0015666), "Semiconductor Integrated Circuit Device, Semiconductor memory System and Clock Synchronous Circuit."

Conclusion

11. Claims 1-21 are rejected as explained above.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

PIERRE BATAILLE
PRIMARY EXAMINER
8/9/06